IN THE CLAIMS

1. (Currently amended) A semiconductor memory device comprising:

a plurality of first bit lines;

a plurality of second bit lines;

a signal generator circuit structured to produce a flag signal notifying a burst read operation;

an address generator circuit structured to provide an address in response to the flag signal;

a column selection circuit structured to select a part of the plurality of first bit lines in response to the addresses, and connect the first bit lines ~~being connected~~ to the plurality of second bit lines, respectively; and

a discharge circuit for discharging voltages from the plurality of second bit lines in response to the flag signal.

2. (Original) The memory device of claim 1, wherein the signal generator circuit is structured to produce the flag signal notifying a next burst read operation after an input of an initial address.

3. (Original) The memory device of claim 1, wherein the signal generator circuit is structured to produce the flag signal synchronized to a clock signal.

4. (Original) The memory device of claim 1, wherein the semiconductor memory device is a NOR type flash memory device.

5. (Original) The memory device of claim 1, wherein the discharge circuit comprises:

a discharge signal generator structured to produce a discharge signal in response to the flag signal; and

a plurality of NMOS transistors respectively connected between the plurality of second bit lines and a ground voltage and controlled by the discharge signal.

6. (Original) The memory device of claim 1, wherein the second bit lines are structured to be discharged before the selecting operation of the column selection circuit.

7. (Currently amended) A semiconductor memory device, comprising:

a plurality of first bit lines, each of which is coupled with a plurality of memory cells;

a plurality of second bit ~~lines~~ lines;

a signal generator circuit for generating a flag signal indicating a burst read operation in response to a clock signal and a chip enable signal;

an address generator circuit for generating addresses in response to the flag signal;

a first column selection circuit for selecting a part of the plurality of first bit lines in response to a first address of the address, the selected first bit lines thus being connected to the plurality of second bit lines respectively;

a discharge circuit for discharging the plurality of second bit lines in response to the flag signal;

a second column selection circuit for selecting a part of the plurality of second bit lines in response to a second address of the address;

a sense amplification control circuit for generating sense amplification control signals in response to a transition of the address; and

a sense amplification circuit for sensing and amplifying voltages of the selected second bit lines in response to the sense amplification control signals during the burst read operation.

8. (Original) The memory device of claim 7, wherein the signal generator circuit generates the flag signal indicating a burst read operation after an input of an initial address.

9. (Original) The memory device of claim 7, wherein the semiconductor memory device is a NOR type flash memory device.

10. (Original) The memory device of claim 7, wherein the discharge circuit comprises:

a discharge signal generator for generating a discharge signal in response to the flag signal; and

a plurality of NMOS transistors respectively connected between the second bit lines and a ground voltage and controlled by the discharge signal.

11. (Original) The memory device of claim 7, wherein the second bit lines are discharged before the selecting operation of the column selection circuit.

12. (Original) A non-volatile semiconductor memory device, comprising:

a plurality of sectors each including a plurality of local bit lines;

a burst enable circuit for generating a burst enable signal in response to a chip enable signal and a clock signal;

a burst read control circuit being operable in synchronization with the clock signal, and for generating a count-up pulse signal in response to the burst enable signal;

an address generator circuit for generating an address in response to the count-up pulse signal;

a first column selection circuit for selecting one of the plurality of sectors in response to a first address of the address and selecting a part of local bit lines of the selected sector;

a plurality of global bit lines respectively connected to local bit lines selected by the first column selection circuit; and

a discharge circuit for discharging voltages of the plurality of second bit lines in response to the flag signal.

13. (Original) The non-volatile memory device of claim 12, further comprising:

a second column selection circuit for selecting a part of the global bit lines in response to a second address of the address;

a sense amplification control circuit for generating sense amplification control signals in response to a transition of the address; and

a sense amplification circuit for sensing and amplifying voltages of the selected global bit lines in response to the sense amplification control signals.

14. (Original) The non-volatile memory device of claim 12, wherein the burst read control circuit generates the count-up pulse signal in response to the burst enable signal to enable a burst read operation after an input of an initial address.

15. (Original) The non-volatile memory device of claim 12, wherein the non-volatile memory device is a NOR-type flash memory device.

16. (Original) The non-volatile memory device of claim 12, wherein the discharge circuit comprises:

a discharge signal generator for generating a discharge signal in response to the count-up pulse signal; and

a plurality of NMOS transistors respectively connected between the global bit lines and a ground voltage and controlled by the discharge signal.

17. (Original) The non-volatile memory device of claim 13, wherein the global bit lines are discharged before the selecting operations of the first and second column selection circuits.

18. (Original) A method of operating a non-volatile memory device including a sector having a plurality of a local bit lines and a plurality of global bit lines connected to a part of the plurality of local bit lines, comprising:

activating a count-up pulse signal synchronized with a clock signal during a burst read operation;

generating an address in response to the activation of the count-up pulse signal;

discharging the global bit lines in response to the activation of the count-up pulse signal; and

after the global bit lines are discharged, selecting the local bit lines and the global bit lines in response to the address.

19. (Original) A method of reading cells in a non-volatile memory device, comprising:

generating a count-up pulse signal;

discharging one or more bit lines in the memory device after receiving the count-up pulse signal;

generating a new address after receiving the count-up pulse signal;

decoding the new address to determine which memory cells of the memory device to read; and

sensing the cells located at the new address using the previously discharged one or more bit lines.

20. (Original) The method of claim 19 wherein discharging one or more bit lines comprises discharging one or more global bit lines.

21. (Original) The method of claim 19, further comprising generating a global discharge signal after receiving the count-up pulse signal.

22. (Original) The method of claim 21, further comprising applying the global discharge signal to a control terminal of one or more switches respectively coupled between the one or more bit lines and a reference voltage.